SPDT 10W/50W$_{peak}$ Power Switch 300 MHz to 8.5 GHz

Features

- Frequency Range 300 MHz to 8.5 GHz
- Low insertion loss:
  0.35 dB @ 2.0 GHz
  0.40 dB @ 4.0 GHz
  0.45 dB @ 6.0 GHz
- High isolation S_{32}:
  46 dB @ 2.0 GHz
  34 dB @ 4.0 GHz
  28 dB @ 6.0 GHz
- 10 W CW Power, 50 W_p Peak Power
- Fast switching time 120 ns
- Low power consumption, less than 1 mW
- No external DC blocking capacitors on RF lines
- All RF ports OFF state
- Versatile 2.6...5.25 V power supply
- No need to supply negative voltages

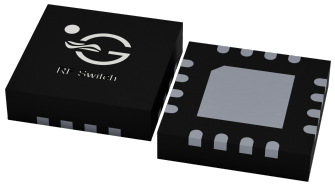


Figure 1: TS8223K in 3.0 x 3.0 mm^2 QFN 16-pin package.

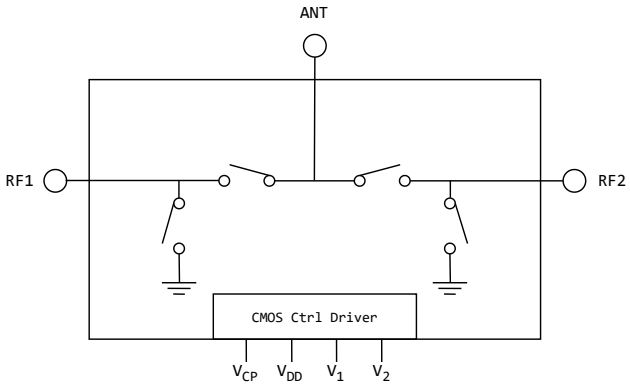


Figure 2: TS8223K functional diagram

RoHS/Reach/Halogen free

Applications

- Drone datalinks
- Private mobile and defense radios
- Public safety handsets
- Cellular infrastructure
- Datalinks

General Description

The TS8223K is a 3rd Generation symmetrical reflective Single Pole Dual Throw (SPDT) switch designed for medium power switching applications. The TS8223K covers 300 MHz to 8.5 GHz bandwidth and provides low insertion loss, high isolation, and high linearity within a small package size. The TS8223K is a 10 W CW with peak power capability of 50 W, switch suitable for applications requiring low insertion loss, high isolation, and high linearity.

The TS8223K is packaged into a compact Quad Flat No lead (QFN) 3.0x3.0 mm^2 16-leads plastic package.

Ordering information

Table 1: Ordering Information

Device Part Number	Package Type	Notes
TS8223K	16 Pin 3.0x3.0x0.85 mm^3 QFN	Core part number
TS8223K-EVB	Evaluation Board	
TS8223KMTRPBF[1]	330 mm reel, 3 000pcs	Full reel

[1] MTRPBF - M: Manufacturing, TR: Tape and Reel, and PBF: lead free.

Table 2: Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3 000	13” (330mm)	18mm

Pin Assignment

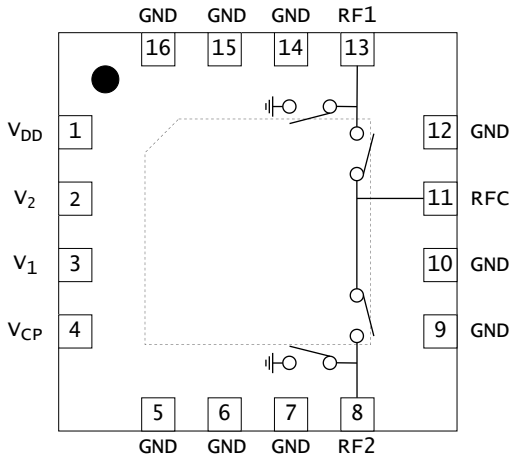


Figure 3: TS8223K pin assignment [top view]

Table 3: Pin Definition

Pin Number	Pin Name	Decription
1	V_{DD}	DC Power Supply
2	V_2	Switch control input 2
3	V_1	Switch control input 1
4	V_{CP}	Internal charge pump voltage output, connect a C_{VCP} capacitor to GND on this node.
5,6,7,9,10,12,14,15,16	GND	Connect to ground[2]
8	RF2	RF port 2
11	RFC	RFC port (antenna port)
13	RF1	RF port 1
17 [1]	GND	Ground thermal pad, please connect to GND

[1] The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias, and adequate heat sinking must be used to ensure proper operation and thermal management.
[2] These pins are NC pins inside the package. To avoid floating pins around RF lines, we request these to be connected to ground.

Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings $T_A = +25$°C unless otherwise specified[1].

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	V_{DD}	5.5	V
Storage Temperature Range	T_{st}	-55...+125	°C
Operating Temperature Range	T_{op}	-40...+85	°C
Maximum Junction Temperature	T_j	+140	°C
Maximum RF CW input power[3]	RFx/RFC	41	dBm
Maximum RF peak input power, 1% duty cycle, 10μs pulse [2]	RFx/RFC	48	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta jc}$	9.9	°C/W
Soldering Temperature	T_{solder}	+260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500...<1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	

[1] Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and can cause permanent damage to the device. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit. Functional operation of the device is not implied in any conditions above those indicated in the Electrical Specifications section.
[2] Test frequency 800MHz.
[3] See Power De-rating table for low frequencies.

Electrical Specifications

Table 5: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	300		8500	MHz
Insertion loss	500 MHz		0.30		dB
unmatched, upto 8.5GHz	2.0 GHz		0.35		dB
$RFC - RFx$	4.0 GHz		0.40		dB
	6.0 GHz		0.45		dB
	8.5 GHz		0.50		dB
Isolation	500 MHz		50		dB
unmatched, upto 8.5GHz	2.0 GHz		37		dB
$RFC - RFx$	4.0 GHz		30		dB
	6.0 GHz		25		dB
	8.5 GHz		19		dB
Isolation	500 MHz		60		dB
unmatched, upto 8.5GHz	2.0 GHz		46		dB
$RF1 - RF2$	4.0 GHz		34		dB
RF1ON	6.0 GHz		28		dB
	8.5 GHz		23		dB
Isolation	500 MHz		58		dB
unmatched, upto 8.5GHz	2.0 GHz		43		dB
$RF1 - RF2$	4.0 GHz		33		dB
RF2ON	6.0 GHz		26		dB
	8.5 GHz		22		dB
Isolation[1]	500 MHz		tbd		dB
Isolation state	2.0 GHz		tbd		dB
$RF1 - RF2$	4.0 GHz		tbd		dB
	6.0 GHz		tbd		dB
	8.5 GHz		tbd		dB

[1] Matched values are not guaranteed as they include performance of matching components. These components are beyond control of TagoreTech and therefore given values are indications, not guaranteed values.

Table 6: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	300		8500	MHz
Return Loss	500 MHz		-25		dB
unmatched, upto 8.5GHz	2.0 GHz		-25		dB
$RFC - RFx$	4.0 GHz		-24		dB
	6.0 GHz		-25		dB
	8.5 GHz		-22		dB

[1] Matched values are not guaranteed as they include performance of matching components. These components are beyond control of TagoreTech and therefore given values are indications, not guaranteed values.

Table 7: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	300		8500	MHz
Harmonic Distortion					
H_2	800MHz, P_{in} =40dBm		tbd		dBc
H_3	800MHz, P_{in} =40dBm		tbd		dBc
IIP3	800MHz		tbd		dBm
Power and Compression point					
P_{maxCW}[2]	Max RF CW Power		40		dBm
P_{maxpeak}	Max RF Peak Power		47		dBm
$P_{\text{maxhot RFx}}$[5]	Max RF CW Power, hot switching		tbd		dBm
$P_{\text{maxhot RFC}}$[5]	Max RF CW Power, hot switching		tbd		dBm
$P_{0.1\text{dB}}$	800MHz, CW		41		dBm
$P_{1\text{dB}}$[1]	800MHz, CW		43		dBm
$P_{\text{peak0.1dB}}$	800MHz, 1% duty cycle, 10μs pulse		47		dBm
Noise					
CP switching noise	RBW=1kHz		-140		dBm
Switching Time					
t_{ON}	Switch ON time		120		ns
t_{OFF}	Switch OFF time		120		ns
t_{RISE}	Switch RISE time		55		ns
t_{FALL}	Switch FALL time		90		ns
t_{wON}	Minimum Switch ON time		1		μs
t_{wOFF}	Minimum Switch OFF time		1		μs
$f_{\text{PRR}}, C_{\text{VCP}} = 1\text{nF}$[3]	Maximum pulse repetition rate		1		kHz
$f_{\text{PRR}}, C_{\text{VCP}} = 10\text{nF}$[3]	Maximum pulse repetition rate		1.4		kHz
$f_{\text{PRR}}, C_{\text{VCP}} = 100\text{nF}$[3]	Maximum pulse repetition rate		1.8		kHz
$f_{\text{PRR}}, V_{\text{CPext}} = -18\,V$[6]	Maximum pulse repetition rate		>20		kHz
$t_{\text{startup}}, C_{\text{VCP}} = 1\text{nF}$[3]	startup time		0.8		ms
$t_{\text{startup}}, C_{\text{VCP}} = 10\text{nF}$[3]	startup time		7		ms
$t_{\text{startup}}, C_{\text{VCP}} = 100\text{nF}$[3]	startup time		40		ms
Power Supply, DC					
Control voltage	Power Supply V_{DD}	2.6	3.3	5.25	V
	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3	0	0.5	V
Control current	All control pins high, I_{ih}			7.5	μA
	All control pins low, I_{il}		0		μA
Current consumption	I_{DD}, active mode (V_{DD} on)		160	260	μA

[1] $P_{1\,\text{dB}}$ has been given for comparison reasons only. Please do not exceed Absolute Maximum ratings.
[2] See Power De-rating table
[3] With internal charge pump and with C_{VCP}.
[5] Dependent on thermal design and surrounding circuits.
[6] External -18 V applied to V_{CP} pin.

Switching time definition

Example of the definition by using 10 W/40 dBm signal. We apply 10W signal to RF port, stabilized with isolator. Isolator is needed as our switch shows to RF port approximately 4Ω impdance. Lets assume that that switch insertion loss is 0.3 dB. Therefore 90% of the RF signal is 39.55 dBm and 10% of the RF signal is 1W/30dBm. We need to take into account 0.3dB insertion loss, therefore numbers are 39.25 dBm and 29.7 dBm respectively. We change the control from low to high and our time reference point is when our control signal exceeds lower threshold value V_{ihlow}. In certain measurements when control signal rise time is significantly shorter than RF output signal, we approximate start of the clock with 50% point of of control signal.

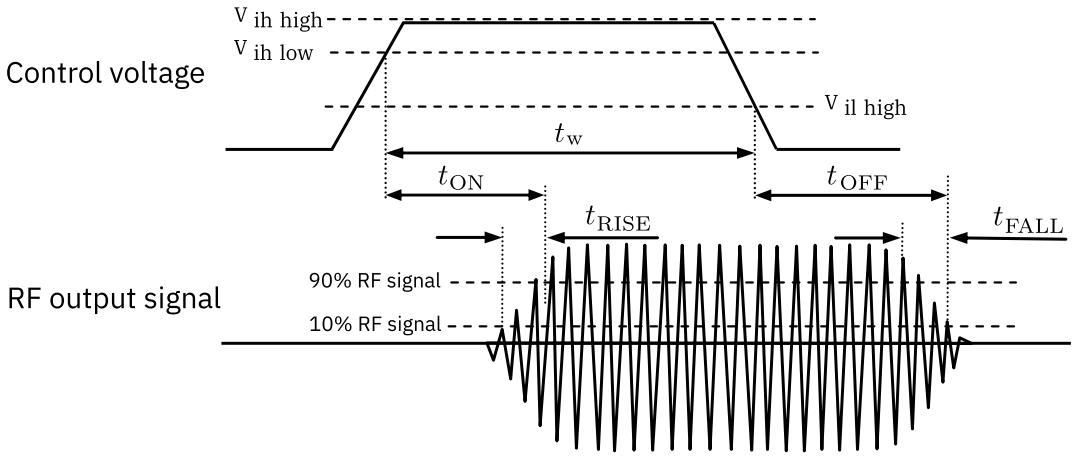


Figure 4: Switching time definition, t_{ON}, t_{OFF}, t_{RISE}, t_{FALL}. Minimum pulse width t_w.

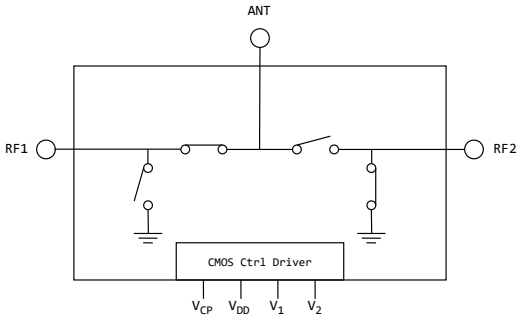
Our component uses integrated charge pump. Maximum pulse repetition rate defines what is maximum frequency for switching events. Please do not exceed given maximum frequency. By feeding external -18 V to V_{CP}, one can improve maximum pulse repetition rate f_{PRR}. Feeding external -18V to V_{CP}, one can drive switch at least to 20kHz f_{PRR}. Expect current consumption of 10mA of -18V.

Switch Control table

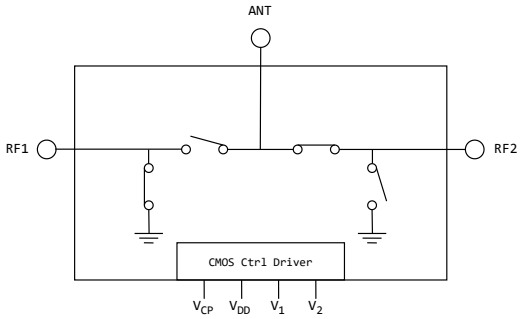
Table 8: Switch Control Table

V_{DD}[1]	V_2	V_1	**Switch state**
1	0	0	$RFC - RF1$ ON[2]
1	0	1	$RFC - RF2$ ON
1	1	0	ISO (Isolation), RFC port open, RF ports shorted[3].
0	0	0	V_{DD} off (Isolation), all FETs are on, short shown to RFC and RF ports

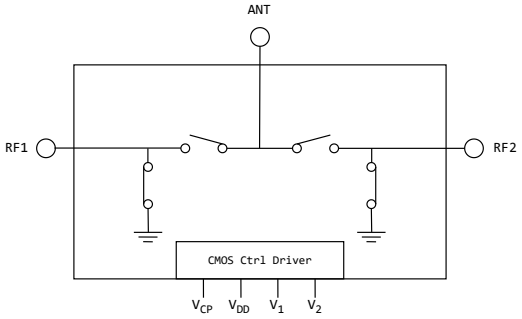
[1] V_{DD} should be applied first before V_1 and V_2, otherwise may cause damage to the device.
[2] There are internal pull-downs to ground on both V_1 and V_2 control pins, the state at start-up without any control voltage applied will be $ANT - RF1$ ON.
[3] If ISO state is not used, the switch can be operated with single control pin V_1



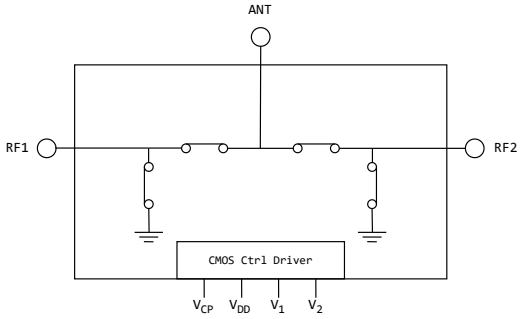
RFC-RF1 ON



RFC-RF2 ON



ISO (Isolation state)



V_{DD} off state

Theory of Operation

Isolation modes

TS8223K has two isolation modes. Both Isolation mode measurements are shown at electrical performance section. Both modes described below.

Device powered off

When V_{DD} is 0V, all switch RF transistors are on, ie. every MOSFET is on. This means that series MOSFETS and shunt MOSETs are conducting. Every RF port is essentially connected to ground, including RFC port. This is practical when device is directly connected to RFC, there is certain protection against induced electrical fields. This can partially protect radio equipment against electrical fields, when device is not in usage. It is important to understand, VDD off mode protects radio frontend during the storage of the radio, against strong signal, which could possibly damage rest of the radio frontend. Moreover, having direct path to ground by switch, provides protection to induced voltages at RFC port.

Device powered, ISO state

In this state, series MOSFETs are OFF, ie. OPEN and shunt MOSFETs are on, ie. closed. RF1 to RF2 isolation is maximum and antenna is completely isolated. ANT port is open, whereas RFx ports are showing effectively short. Low frequency isolation in this case is approximately 60dB as basically there is DC block due to open FETs.

Feeding external V_{CP} voltage of -18 V

TS8223K supports external voltage supply to V_{CP} to increase pulse repetition rate f_{PRR}. With external voltage supply, f_{PRR} can be increased at least to support pulse repetition rate more than 20 kHz, in some cases even up to 100 kHz. In order to use external voltage, it is mandatory to supply first V_{DD}, have a delay of 1 ms and then apply -18 V to V_{CP}. Shutdown should be in opposite order.

Applications

TS8423K is offering 10 W/50 W_{peak} capability from 300 MHz to 8500 MHz frequency band. Applications include narrowband and multi-octave wideband radios, jammers, EMC testing, public mobile radios, industrial and scientific applications. In the past, such applications were covered with power hungry and complex PIN diodes, TS8223K significantly reduces design complexity for such RF switching needs. TS8223K works well upto 8.5 GHz frequency without external matching components.

Schematics and Evaluation Board

S-parameters of the both presented EVBs can be downloaded from link: Download TS8223K S-parameters

Table 9: Port definitions in s-parameter files and plots.

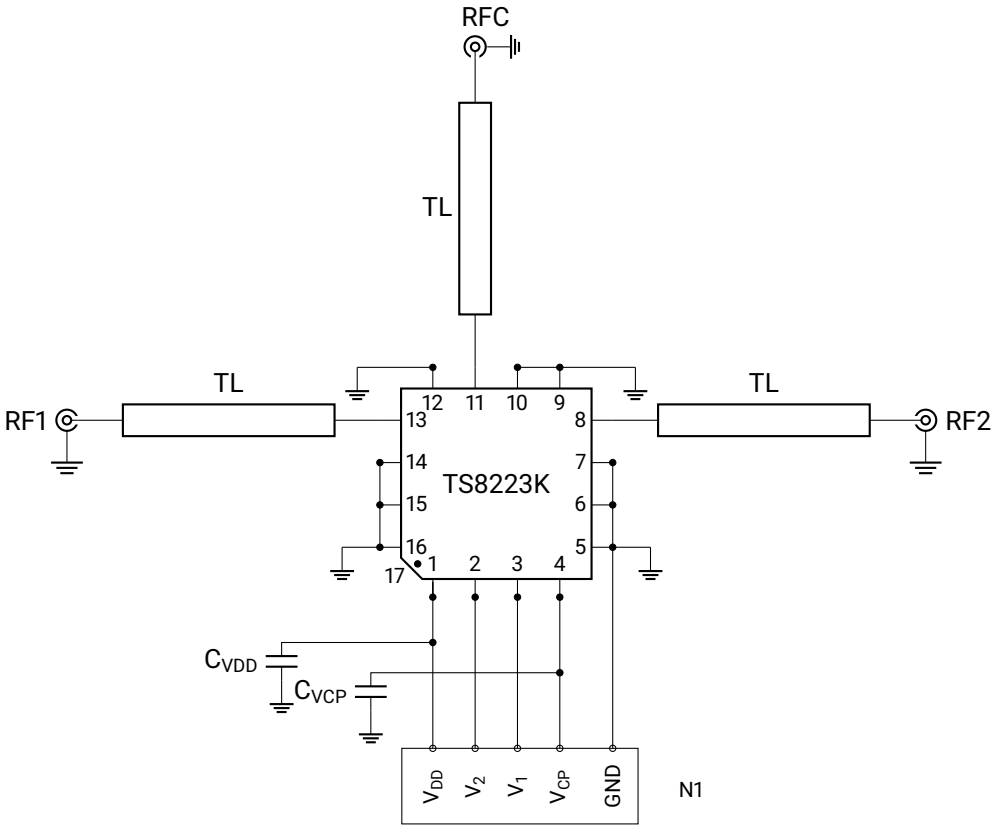
PIN name	Port numbers	S-parameters	Function
RFC	1	S11	
RF1	2	S22	
RF2	3	S33	
RF1ON	12	S21	RFC-RF1 ON
RF2ON	13	S31	RFC-RF2 ON

Content of s-parameter repository:

```
TS8223K.zip
└── IDX_00 ..... Directory for s-parameters without matching components
    ├── Readme.txt
    ├── TS8223K_RF1ON_3PORT.s3p ..... S3P file for ANT-RF1ON mode
    ├── TS8223K_RF2ON_3PORT.s3p ..... S3P file for ANT-RF2ON mode
    ├── TS8223K_ISO_3PORT.s3p ..... S3P file for ISO mode
    └── TS8223K_OFF_3PORT.s3p ..... S3P file for VDD off mode
```

TS8223K EVB

TS8223K shows best performance upto 8.5 GHz frequency without any matching components. Only two external components are recommended, 1 nF for V_{CP} and 10nF forV_{DD} lines.



Schematics of TS8223K EVB

Table 10: Components used for TS8223K EVB

Reference	Part number / Value	Description	Notes
C_{VDD}	10nF	Capacitor	
C_{VCP}	1nF	Capacitor	

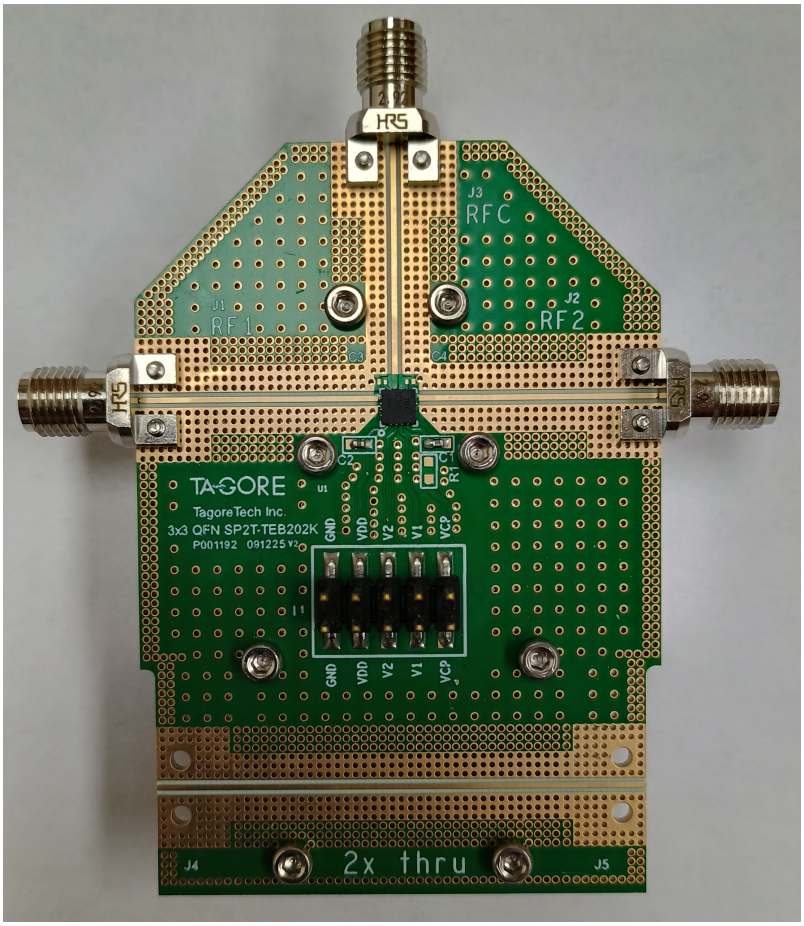
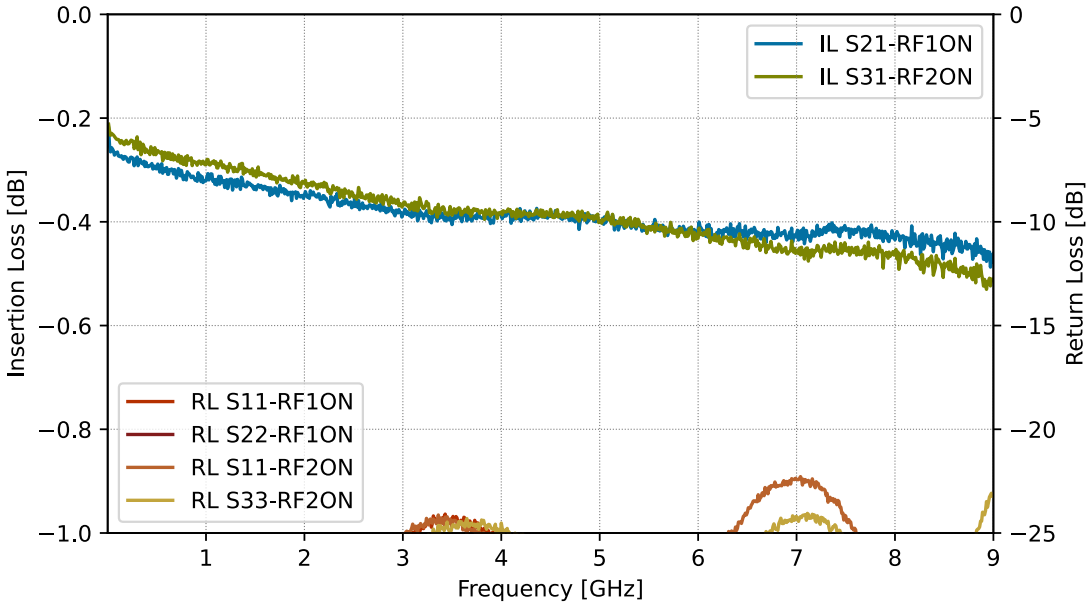


Photo of TS8223K EVB

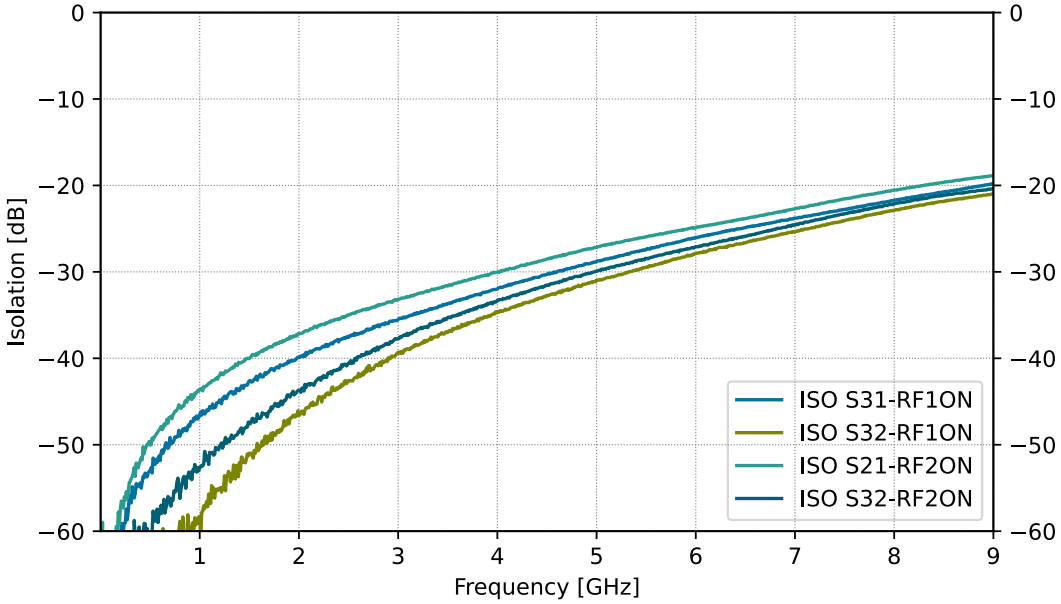
Typical characteristics

Performance upto 8.5 GHz

These measurements have been taken from TS8223K EVK, CPW losses have been de-embedded from the measurements. Device does not require any matching components for operation upto 8.5 GHz. Return loss for whole frequency range is better than -22 dB. To keep consistency with TagoreTech other datasheets, y-axis of return loss is set to -25 dB. Matching is excellent as RL curve is hardly visible.

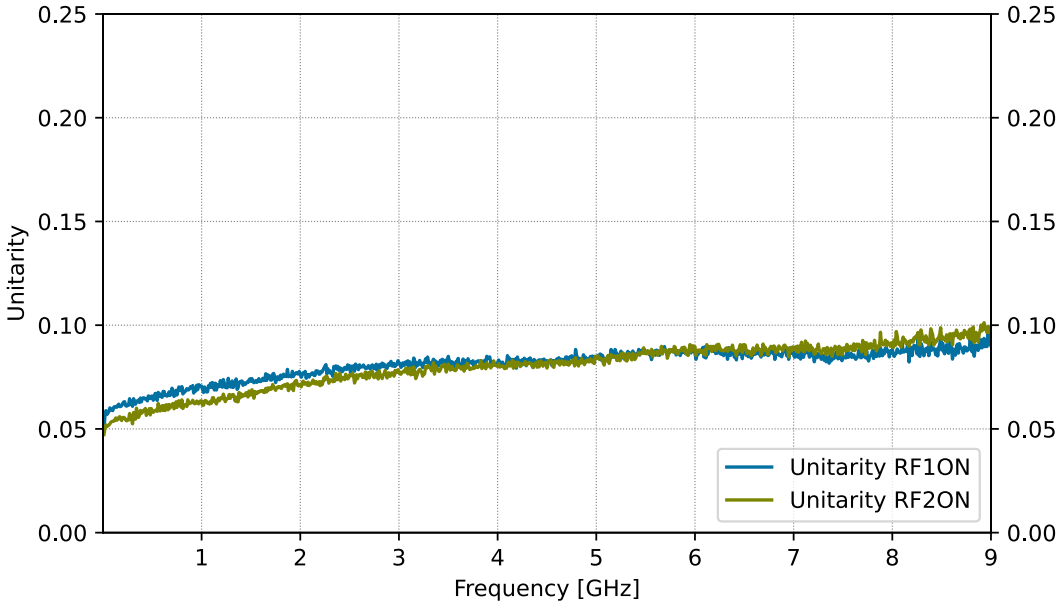


Insertion loss and Return loss, RFC – RFx.

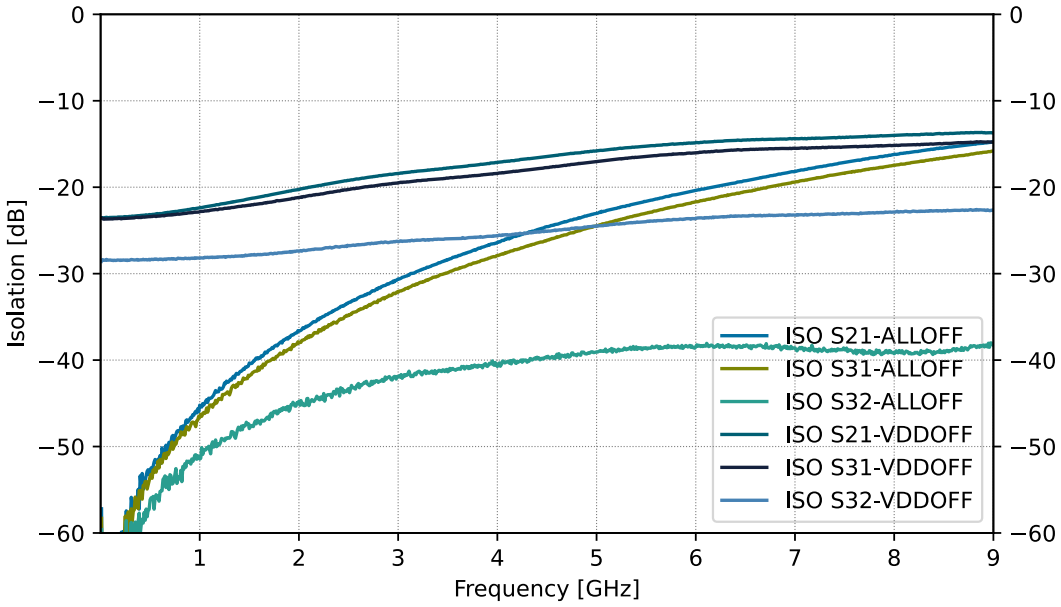


Isolation between RFC to non-active RFx and active RFx to non-active RFx.

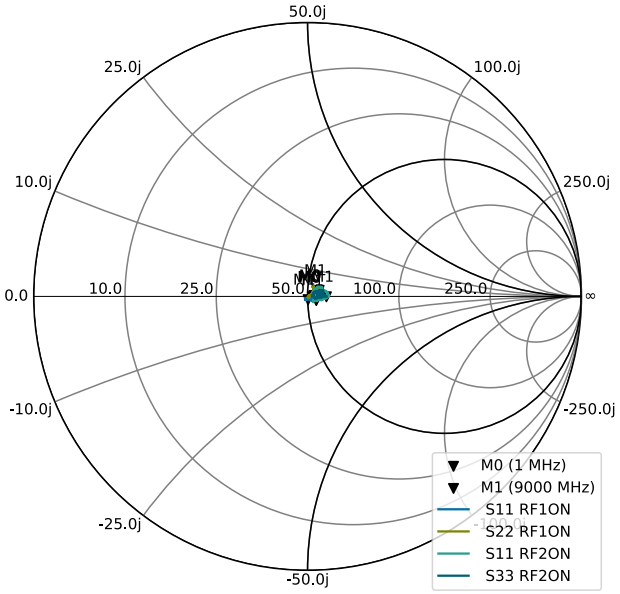
Unitarity, ie. power absorption of the switch describes power absorption of the switch and required cooling. In case of 20W input power, and power absorption of 0.07 means that 1.4 W is converted to heat.



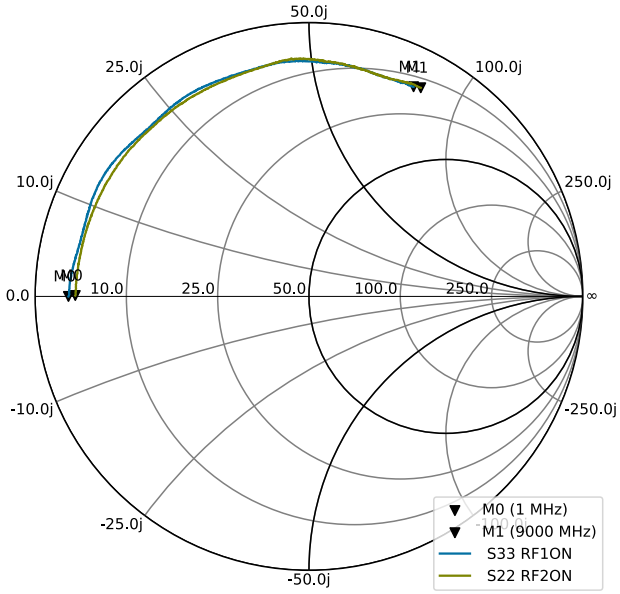
Power absorption of the switch $1 - |S_{11}|^2 - |S_{21}|^2 - |S_{31}|^2$, $\mathrm{RFC} - \mathrm{RFx}$.



$\mathrm{RFC} - \mathrm{RFx}$ and $\mathrm{RF1} - \mathrm{RF2}$ isolation at ISO mode and $\mathrm{V_{DD}}$ off (Isolation).



Active RFx and RFC port impedance



Non-active RF1 and RF2 termination impedance

Device Package information

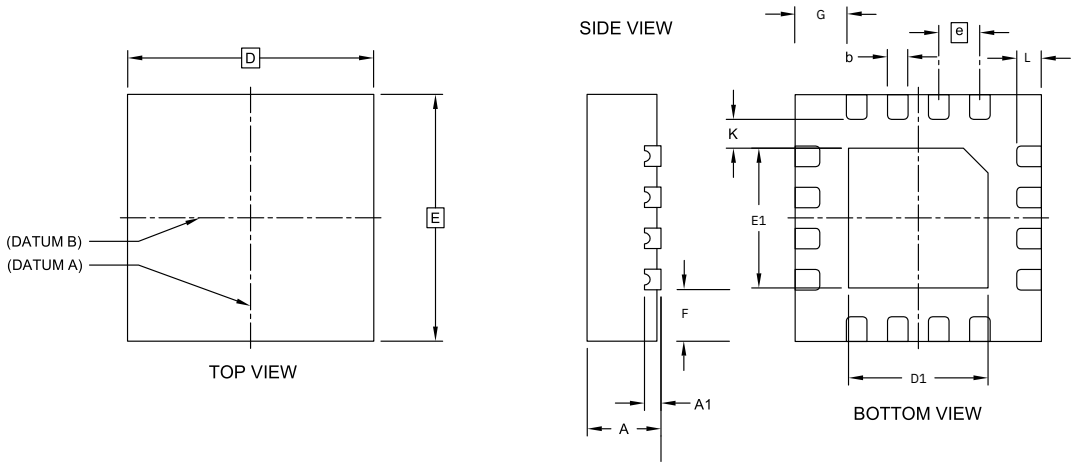


Figure 7: 16-pin QFN 3.0 x 3.0 x 0.85 mm^3 package drawing.

Please refer to application notes TN-001 and TN-002 at TagoreTech web page for PCB and soldering guidelines.

Table 11: Device Package Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A	0.85	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

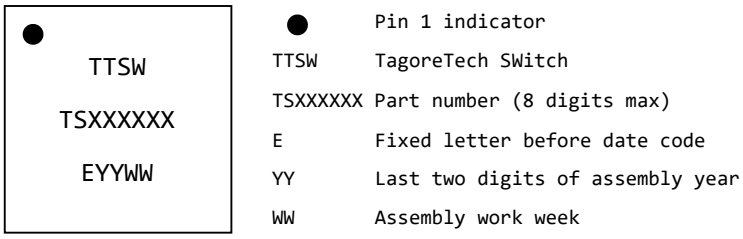


Figure 8: Part marking specification.

PCB Land Design

Notes:

- 4-layer PCB is recommended.
- Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias.
- Thermal vias shall only be placed on the center pad.
- The maximum via number for the center pad is 11(X)×11(Y)=121.

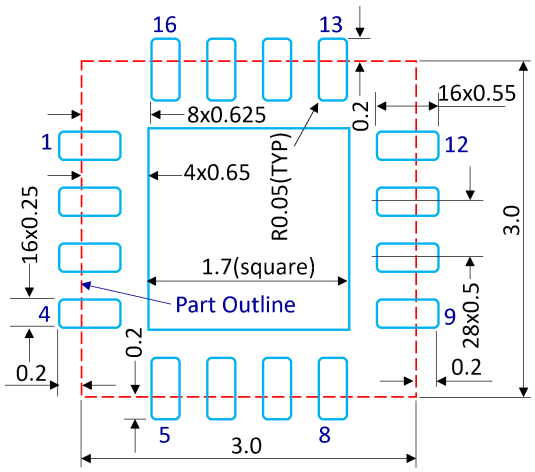


Figure 9: PCB land pattern, dimensions in [mm].

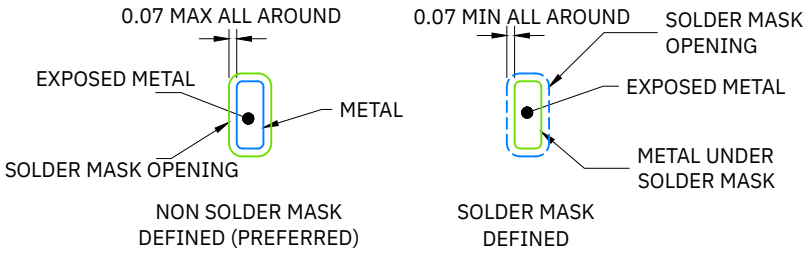


Figure 10: Solder mask opening, dimensions in [mm].

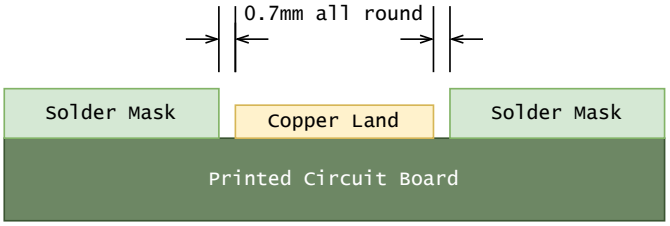


Figure 11: Preferred solder mask opening, side view, dimensions in [mm].

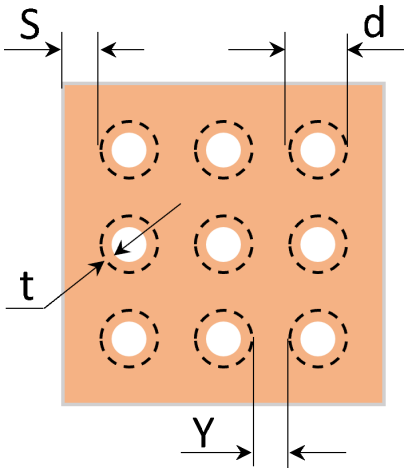


Figure 12: Thermal Via Pattern, Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm.

PCB Stencil Design

Notes:

- Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- Stencil thickness is recommended to be 125μm.

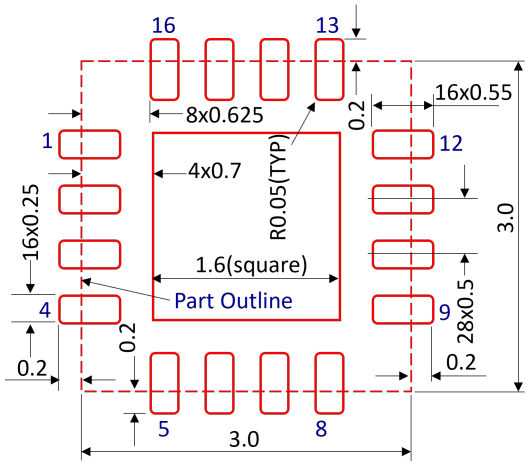


Figure 13: Stencil Openings, dimensions in [mm].

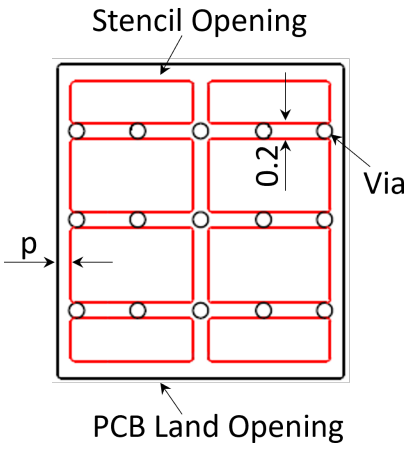
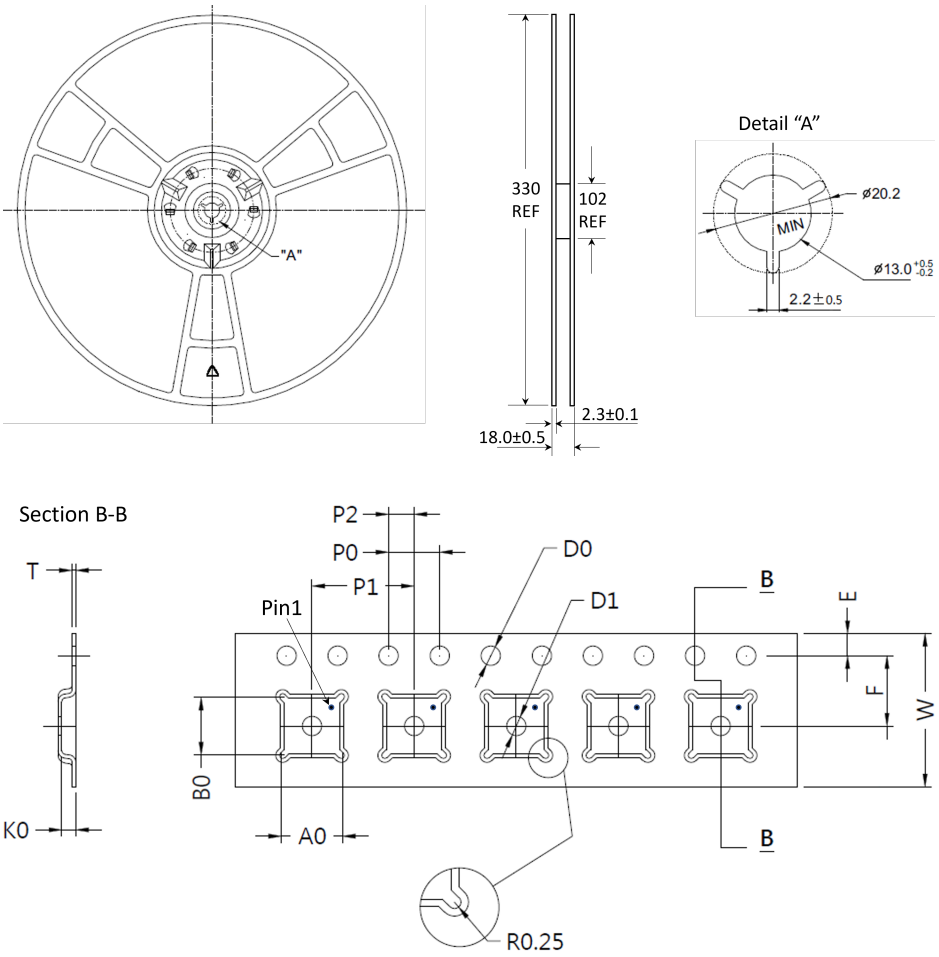


Figure 14: Stencil Openings Shall not Cover Via Areas If Possible, dimensions in [mm].

Tape and Reel Information



A0[mm]	B0[mm]	D0[mm]	D1[mm]	E[mm]	F[mm]	K0[mm]	P0[mm]	P1[mm]	P2[mm]	T[mm]	W[mm]
3.30	3.30	1.50	1.50	1.75	5.50	1.10	4.00	8.00	2.00	0.30	12.00

Glossary

IL	Insertion loss
ISO	Isolation
RL	Return loss
VSWR	Voltage Stading Wave Ratio
RFC	RF Common port, sometimes referred as ANT
RFx	RF Port number x
Unitarity	Describes power absorption of the component, $1 - \|S_{11}\|^2 - \|S_{21}\|^2 - \|S_{31}\|^2$

Changelog

Table 12: Changelog

Date	Revision	Notes
11/05/2025	0.1	First release of Product Brief
11/08/2025	0.11	Pin-out added
02/15/2026	0.9	First Preliminary datasheet

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